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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/389,321    09/03/99    HIRAMOTO

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EXAMINER

021839    MM92/0209  
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

# Office Action Summary

Application No.

09/389,321

Applicant(s)

HIRAMOTO ET AL.

Examiner

Thomas L Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6
- 18) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_

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## DETAILED ACTION

### *Oath/Declaration*

1. The oath/declaration filed on 09/03/98 is acceptable.

### *Drawings*

2. The drawings are objected to by the PTO Draftsperson for the reasons noted on the attached Notice of Draftsperson's Patent Drawing Review, form PTO-948.

### *Priority*

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

4. The Information Disclosure Statement filed on August 2, 1996 has been considered.

It is noted that the German and French patents have been considered to the best of the ability of the examiner without benefit of translation.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the in-

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vention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Applicant's specification makes the following definitions:

1. MOS and DTMOS are defined as generally understood, where a DTMOS has a gate, oxide gate insulator, channel region, and an electrical connection between the gate and the channel region. Application at p. 2 ll. 12-24.
2. EIB, electrically induced body, or EIB-MOS, is an SOI MOS adapted for biasing the voltage of the substrate relative to the body, i.e. channel region. Application at p. 9, ll. 7-11. For brevity, the examiner has adopted this terminology and will refer to a EIB-FET as a FET, either MOS or junction, adapted for biasing the voltage of the substrate relative to the body.
3. VT MOS is an EIB-MOS where the substrate voltage bias may be switched from a first voltage to a second, lower bias. Application at p. 2, ll 7-11.
4. Accumulation mode means a FET with its channel having the same conductivity as its drain and source.

Claims 1, 2, and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over BURR et al. (6,100,567).

With regard to claims 1 and 5, Burr discloses a complementary FET (field effect transistor) comprising an SOI (502, 504) which includes a substrate (552, 554) com-

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posed of a semi-conducting material, a single crystal semi-conducting layer (512, 514, 516 or 520, 522, 524), an insulating oxide substrate (508) where the semi-conducting layer (512, 514, 516), is made of a source (512, 520), drain (514, 522), and a surrounded region (516, 524) that is surrounded by the source (512, 520) and the drain (514, 522). Burr further discloses a connection (544, 546) that adapts the substrate (540, 542) to be applied with a voltage of a first polarity, and a depletion region, i.e. a depletion layer (328). Note figs. 3, 5, and col. 1, l. 27.

Burr does not teach an MOS because Burr does not explicitly show a metal gate, or an oxide insulating that gate from the surrounded region. Rather Burr teaches a conductive polysilicon layer that functions as a gate, with no particular means specified for achieving the gate. Further, Burr does not teach a composition surface in the depletion layer that is in contact with the insulating layer and in which charges of a second polarity are induced.

However, the poly gate of Burr is recognized as the equivalent of a metal gate. Further, it would be clear that an insulator could be placed between the transistor body and Burr's gate to form an FET of the MOS type. In context, the "composition surface" is the depletion layer surface in contact with the insulating layer. One skilled in the art would understand that applying a voltage to the conductive substrate would cause all surfaces, including the one opposing the composition surface, to have that voltage. One skilled in the art would further understand that when placed in opposition to a surface having voltage of first polarity, the surface of a conductive body such as the depletion

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layer would carry charges of second polarity. Therefore, it would be obvious to one of ordinary skill in the art to build an FET of the MOS type according to the teachings of Burr, in order to obtain the advantages of an FET with variable threshold voltage taught by Burr. It would be obvious that that FET would include a composition surface in the depletion layer in contact with the insulating layer in which charges of a second polarity are induced.

With regard to claim 2, Burr teaches an DT-FET where the undepleted channel region is electrically connected to the gate. With an oxide layer between gate and channel, this FET would be a DTMOS transistor. See fig. 2, esp. part 230. It would have been obvious to one of ordinary skill in the art to combine Burr's DT-FET with Burr's EIB-FET and place an insulator between the transistor body and Burr's gate to form an DT-FET of the MOS type in order to combine the voltage threshold reduction realized by the DT-FET, as taught by Burr, with the variable threshold voltage advantages of the EIB-FET, as taught by Burr.

With regard to claim 4, the examiner does not read a patentable weight into the distinction between "EIB-MOS" and VT MOS. Applicant defines EIB as a MOS with a voltage adapted to be applied to the substrate, said voltage inducing a "mirror" charge in the body. Application, p. 9, ll 7-11. It is clear that applicant believes that the "mirror" charge controls the effective channel depth and thus the threshold voltage

Applicant defines VT MOS as a transistor in which the threshold voltage is controlled by "(the) whole of a chip" in which the VT MOS transistor is provided, or alterna-

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tively, as a transistor where a first voltage is applied to the substrate in the "active mode," and a second, smaller, voltage is applied in the "standby mode."

"Whole of the chip," "active mode," and "standby mode," lack written description and enablement and therefore may not be used in the claims. For this reason, VT MOS, which is used in the claims, may not be defined in a way that imports these terms into the claims. Without using these terms, a VT MOS is a transistor where a first voltage is applied to the substrate and (alternatively) a second, smaller, voltage is applied. A VT MOS, so defined, would have been obvious to one of ordinary skill in the art under the same analysis used for the EIB-MOS.

With regard to claim 6, Burr teaches the step of applying a voltage of a first polarity to the substrate of an EIB-FET, and that this step controls the threshold voltage. See Burr, col. 6 table 1. For this reason, it would have been obvious to one of ordinary skill in the art to perform the same step with a EIB-MOS which includes a semiconducting substrate, a semiconducting single crystal layer, an insulating oxide interposed between, source, drain and surround regions, depletion layer and composition surface, in order to tune the performance of the FET, as taught by Burr.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of WARASHINA, et al. (5,698,885)

Burr discloses an EIB-FET with all the limitations of claim 3 except the MOS gate structure, composition surface, induced charges of second polarity, and accumulation mode, i.e. channel having same conductivity as introduced carriers. Warashina et

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al. discloses a MOS FET in accumulation mode. The MOS FET is known to reduce power by limiting gate current. Accumulation mode is described by Warashina et al. as reducing power by reducing threshold voltage. Burr describes the EIB-FET as reducing power by reducing threshold voltage. Therefore, it would have been obvious to one of ordinary skill in the art to combine the MOS-FET of Warashina et al. with the EIB-FET of Burr, in order to reduce power consumption.

### ***Conclusion***

6. Papers related to this application may be submitted to Technology Center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 3-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2826 Fax Center number is (703) 308-7722 and 308-7724. The Group 2800 Fax Center is to be used only for papers related to Group 2800 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to Thomas Dickey whose telephone number is **(703) 308-0980**. The Examiner is in the Office generally between the hours of 8:00 AM to 5:00 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**.

  
**Minh Loan Tran**  
**Primary Examiner**